IN THE SPECIFICATION

Please replace the first paragraph on page 3 with the following:

U.S. Patent 6,123,862 to Donohoe et al discloses an etching process for high aspect ratio openings. U.S. Patent 6,156,643 to Chen et al teaches a dual damascene process. U.S. Patents 6,159,661 to Huang et al, 6,096,655 to Lee et al, and 6,127,089 to Subramanian et al show dual damascene processes using low dielectric constant materials.

A1

IN THE CLAIMS

Please amend the Claims as follows:

1. (AMENDED) A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

A2

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein no portion of said dielectric layer has a dielectric constant higher than 2.5;